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EXAMINER	
FAN, CHIEH M	

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2638	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/510,861	TAMURA, KOICHI	
	Examiner	Art Unit	
	Chieh M. Fan	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/9/05.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) 11-14 and 25-28 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5,9,10,15-19,23,24,29,30 is/are rejected.

7)☒ Claim(s) 6-8 and 20-22 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 February 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed 06/09/2005.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 29 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Namiki (U.S. Patent No. 4,057,762).

Regarding claim 29, Namiki teaches a demodulation circuit (Fig. 4) comprising: a receiver, which receives a signal (1000 in Fig. 4) including a known signal and outputs a digital transmission signal; a demodulator (1001, 1002, 1003 in Fig. 4), which demodulates said digital transmission signal and outputs a base band signal; an analog-to-digital (A/D) converter (1004, 1006 in Fig. 4), which converts said base band signal; a comparing circuit (3001, 3002, 3005, 3006 in Fig. 4), which compares said known signal with a stored signal (406 in Fig. 4); and a phase shifter, which shifts a phase of one of said digital transmission signal and said base band signal on the basis of the result of comparison made by said comparing circuit (1007 in Fig. 4; col. 2, lines 12-16; col. 5, lines 62-67; col. 6, lines 67-68; that is, the control signal passing through element 1007

phase-shifts the phase of the local carrier generated by the oscillator 1006, which in turn phase-shifts the phase of the digital transmission signal (input to 1001, 1102) and consequently the phase of the baseband signal (output of 1001, 1002)).

Regarding claim 30, Namiki teaches a demodulation method (Fig. 4) comprising: receiving a signal (1000 in Fig. 4) including a known signal and outputting a digital transmission signal; demodulating (1001, 1002, 1003 in Fig. 4) said digital transmission signal and outputting a base band signal; converting said base band signal using an analog-to-digital (A/D) converter (1004, 1006 in Fig. 4); comparing (3001, 3002, 3005, 3006 in Fig. 4) said known signal with a stored signal (406 in Fig. 4); and shifting a phase of one of said digital transmission signal and said base band signal on the basis of the said comparing (1007 in Fig. 4; col. 2, lines 12-16; col. 5, lines 62-67; col. 6, lines 67-68; that is, the control signal passing through element 1007 phase-shifts the phase of the local carrier generated by the oscillator 1006, which in turn phase-shifts the phase of the digital transmission signal (input to 1001, 1102) and consequently the phase of the baseband signal (output of 1001, 1002)).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 17, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. (U.S. Patent No. 5,991,344, cited in previous Office Action dated 11/17/03, "Fujii" hereinafter) in view of the admitted prior art and Sasaki et al. (U.S. Patent No. 3,461,274, hereinafter "Sasaki").

Regarding claim 3, Fujii teaches a demodulation circuit (250, 270 through 157, 158 to 210 in Fig. 1) for demodulating a digital transmission signal having improved power consumption for an A/D converting means further comprises orthogonal demodulating means (156 in Fig. 1) for performing orthogonal demodulation of said digital transmission signal,

said A/D converting means includes two A/D converters (157, 158 in Fig. 1) for two base band signals demodulated by the orthogonal demodulation means,

symbol judgment portion (213 in Fig. 1) for making judgment of symbols of digital signals output from the A/D converters,

automatic frequency controlling (AFC) means including P/S converter (214 in Fig. 1) for converting the output signal of the symbol judgment portion, comparing portion (230 in Fig. 1; note that 230 is a unique word (UW) detector) for comparing the known signal extracted from the output signal of the P/S converter with the known signal inserted at the transmitting end, and a controller (220 in Fig. 1) for repeatedly controlling the frequency of a local oscillator (VCO 164 in Fig. 1) before digital conversion by said A/D converting means on the basis of a result of comparison by the comparing portion (220 in Fig. 1; note that, as shown in Fig. 1, the controller 220 sends a control signal to the VCO 164, which in turn controls the phase of the demodulators 270, 280 and 156;

also note that the phase is controlled or adjusted before the A/D converting means) so as to achieve frequency synchronization.

Fujii does not show that (a) the detail of a UW detector 230 and (b) the AFC means phase-shifts the baseband signal or the digital transmission signal.

With respect to item (a), Sasaki teaches a UW detector that compares the received UW with the UW stored in a register so as to detect the UW. Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that the UW detector of Fujii compares the received UW signal with the UW signal stored in the receiver so as to detect the UW signal.

With respect to item (b), the admitted prior art teaches that the frequency offset between transmission and reception causes phase shift of the input signal of the A/D converter from a desired sampling timing (page 3, line 21 through page 4, line 1; also see page 1, lines 13-17). Therefore, it is clear that the reduction of frequency offset between transmission and reception equivalently shifts the phase of the input signal of the A/D converter to the desired sampling time. The AFC means and the phase shifting means are functionally equivalent. The selection of any one of the two equivalents to ensure the A/D converter to sample at the desired sampling timing would be within the level of ordinary skill in the art.

Claim 17 is the corresponding method claim of claim 3, and is therefore rejected for the same reason above.

Regarding claims 29 and 30, claims 29 and 30 recite similar limitations as claim 3 except the removal of the P/S converter and orthogonal demodulation. Claims 29 and 30 are also rejected for the same reason above.

5. Claims 4 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al. (U.S. Patent No. 5,991,344) in view of the admitted prior art and Sasaki et al. (U.S. Patent No. 3,461,274, hereinafter "Sasaki") as applied to claims 3 and 17 above, and further in view of Miya et al. (U.S. Patent No. 5,572,516, cited in previous Office Action dated 11/17/03, "Miya" hereinafter).

Regarding claims 4 and 18, Fujii in view of admitted prior art and Sasaki teaches the claimed invention (see the rationale applied to claims 3 and 17 above), but does not teach reception data processing portion obtaining an information data by removing the known signal.

Miya teaches a frame decomposition circuit (124 in Fig. 1) that reproduces the information by removing the unique word (col. 6, lines 28-32).

It is known that the unique word does not contain any information and is generally only used for synchronization purpose. It is therefore required to remove the unique word from the received signal in order to obtain the information. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate a reception data processing portion that removes the known signal to obtain the information data, since the known signal does not contain any information.

6. Claims 1, 2, 5, 9, 15, 16, 19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al. (U.S. Patent No. 5,920,220, hereinafter "Takao") in view of Spagnoletti et al. (U.S. Patent No. 6,151,356) and Horii et al. (WO 98/56148, cited previously "Horii" hereinafter; an equivalent U.S. Patent No. 6,693,978 is also cited previously as translation).

Regarding claim 1, Takao teaches a demodulation circuit (see Fig. 4) for demodulating a digital transmission signal having improved power consumption levels and sampling frequency for an A/D converting means wherein

a known signal is inserted in said digital transmission signal at transmission (BTR, UW in Fig. 6(a)),

said demodulation circuit comprising: said A/D converting means (2, 3 in Fig. 4) for performing A/D conversion of a base band signal obtained by demodulation (1 in Fig. 4) of said digital transmission signal; and phase shifting means (7 in Fig. 1) for repeatedly varying a phase shift the sampling clock of said A/D converting means on the basis of a comparison between said known signal after digital conversion by said A/D converting means and said known signal that was inserted at transmission (10 in Fig. 4; the phase estimation circuit 10 control the phase shift of the phase shifting means 7 according to the phase error estimated by sampling the known clock timing recovery signal (BTR), see col. 10, lines 35-65; further note that Takao also teaches the detection of UW signal to control the switch 11, which also loosely meets the claimed limitation).

The difference between Takao and the claimed invention lies in that (a) Takao phase-shifts the sampling clock rather than phase-shifts one of the digital transmission signal and baseband signal and (b) Takao does not particularly teach a parallel-to-serial (P/S) conversion that occurs after the comparison.

With respect to item (a), Spagnoletti teaches that the synchronization between the local clock signal and the incoming data signal may be achieved by placing a phase shifter in the local clock signal path or in the data signal path or both (col. 1, lines 46-57). The selection of any of these three equivalents to achieve synchronization would be within the level of ordinary skill in the art. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to place the phase shifter in the data signal path of Takao to delay one of the digital transmission signal and the baseband signal.

With respect to item (b), the P/S conversion is well known in the art to convert the I and Q components into one output symbol. Horii teach an analogous demodulator that comprises a P/S converter (123 in Fig. 5) that converts the I and Q components into a serial data output. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that a P/S conversion means, as shown by Horii, is coupled to the baseband signal processing circuit of Takao to facilitate the generation of output symbol.

Regarding claims 2 and 5, the demodulation circuit of Takao further comprises orthogonal demodulating means (1 in Fig. 4), A/D converting means including two A/D converters (2, 3 in Fig. 4), symbol detecting means (4 in Fig. 4). Further note that

whether the phase shifting means is used to shift the phase of the baseband signal or the digital transmission signal will produce the same result. The selection of any of these two equivalents to achieve synchronization would be within the level of ordinary skill in the art.

Regarding claim 9, as shown in Fig. 6(a) of Takao, the information data and the known signal are time multiplexed.

Regarding claim 15, claim 15 is the corresponding method claim of claim 1, and is therefore rejected for the reason applied to claim 1 above.

Regarding claim 16, claim 16 is the corresponding method claim of claim 2, and is therefore rejected for the reason applied to claim 2 above.

Regarding claim 19, claim 19 is the corresponding method claim of claim 5, and is therefore rejected for the reason applied to claim 5 above.

Regarding claim 23, claim 23 is the corresponding method claim of claim 9, and is therefore rejected for the reason applied to claim 9 above.

7. Claims 10 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al. (U.S. Patent No. 5,920,220, hereinafter "Takao") in view of Spagnoletti et al. (U.S. Patent No. 6,151,356) and Horii et al. (WO 98/56148, "Horii" hereinafter; an equivalent U.S. Patent No. 6,693,978 is also cited as translation) as applied to claims 1 and 15 above, and further in view of Odenwalder et al. (U.S. Patent No. 6,480,521, cited previously) and Sawahashi et al. (U.S. Patent No. 5,694,388, cited previously).

Takao in view of Spagnoletti and Horii teach the claimed invention (see the rationale applied to claims 1 and 15 above), but does not teach that the information data is transmitted in one of the I and Q channels and the known signal is transmitted in the other of the I and Q channels. However, it is common in the ad that the known signal, such as pilot signal, unique word etc., and the information data are transmitted at separate channels. Odenwalder et al. teach that the pilot signal may be transmitted solely on either the I or Q channels (col. 8, lines 55-56). Sawahashi et al. teach transmitting the pilot signal and the information data on separate channels (Fig. 12). The pilot signal is transmitted continuously on the pilot channel to achieve good tracking ability to the Rayleigh fading (col. 29, lines 17-21). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to transmit the information data on one of the I and Q channels, and transmit the known signal on the other of the I and Q channels, so as to achieve good tracking ability on the Rayleigh fading.

Response to Arguments

8. Applicant's arguments filed 6/9/05 have been fully considered but they are not persuasive.

With respect to the Fujii reference, the applicant argues that *the AFC control and frequency sweeping are different from a phase shift. Although the frequency of the*

oscillator of the demodulator can be controlled, the output of the demodulator cannot be optimized with the phase of sampling signal (see page 15 of the response).

Response --- The applicant admitted in the background section of the instant application that the phase of the input signal to the A/D converter is shifted to cause offset from a desired sampling timing because of the frequency offset appears on the orthogonal demodulation output (see page 3, line 21 through page 4, line 1, also see page 1, lines 13-17). Therefore, the reduction of frequency offset essentially reduces the phase offset from the desired (optimal) sampling timing. The examiner disagrees that the statement, "although the frequency of the oscillator of the demodulator can be controlled, the output of the demodulator cannot be optimized with the phase of sampling signal" may be applied in the instant application. The AFC of Fujii reduces the frequency offset between the transmission and reception and essentially phase-shifts the input signal to the A/D converter toward the optimal sampling timing. Nevertheless, the examiner has changed the rejection of claims under 35 USC 102 to 35 USC 103.

With respect to Fujii, the applicant also argues that Fujii solely detects the unique word when a 1 is detected in the two MSBs. Fujii does not teach the claimed comparison portion, as described in the specification at pages 12-15.

Response --- Fujii teaches that the detection of MSBs in performed by the initial SW detector 312. On the other hand, the unique word detection is performed by the synchronization detector 230, not the initial SW detector. The detection of a 1 in the two MSBs is a condition when the UW detector 230 can detect the unique word (see col. 9, line64 through col. 10, line 6). Therefore, Fujii does not detect the UW by solely

detecting a 1 in the two MSBs. If the system of Fujii is functioned as argued by the applicant, a sole initial SW detector 312 is sufficient to detect the UW. The UW detector 230 would not be required.

Applicant's arguments with respect to the Tarallo reference have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

9. Claims 6-8 and 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Limberg et al. (U.S. Patent No. 6,621,527).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chieh M. Fan whose telephone number is (571) 272-3042. The examiner can normally be reached on Monday-Friday 8:00AM-5:30PM, Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chieh M Fan
Primary Examiner
Art Unit 2638

August 16, 2005